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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,791	12/05/2001	Toshimitsu Tamagawa	103213-00042	2283

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EXAMINER	
VILLECCO, JOHN M	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,791	TAMAGAWA, TOSHIMITSU	
	Examiner	Art Unit	
	John M. Villecco	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,11,13 and 14* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 8, 2006 has been entered.

Response to Amendment

2. Applicant has cancelled all of the previously pending claims (claims 1-8) and added new claims 9-14. Please see the new grounds of rejection for claims 9-14 presented on the following pages.

Claim Objections

3. Claim 11 is objected to because of the following informalities:

- In line 13 of claim 11, applicant recites the phrase "each of the plurality of first groups". However, there is insufficient antecedent basis for this limitation. It is clear that in line 3 of claim 11, applicant meant to use the phrase "divided into a plurality of first groups".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al. (U.S. Patent No. 5,724,094).**

5. Regarding ***claim 9***, Tseng discloses a contact image sensor utilizing differential voltage pickoff. More specifically, Tseng discloses a plurality of image reading photoelectric conversion elements (pixels S_1-S_n and d_1-d_n) divided into a plurality of groups (grouping of the chips as shown in Figure 10); a read selection circuit (shift register, col. 3, lines 54-57) for sequentially selecting the plurality of image reading photoelectric conversion elements and reading a photoelectric conversion signal from the selected image reading photoelectric conversion element; an initialization selection circuit for sequentially selecting the plurality of image reading photoelectric conversion elements and initializing the selected image reading photoelectric conversion element (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel, col. 3, lines 59-60) ; a plurality of signal output lines by way of which the photoelectric conversion element signal is transmitted, each of the plurality of signal output lines corresponding to and independently provided for each of the plurality of groups (as shown in Figure 10 each of the chips has an output line through which the

photoelectric signal is transmitted); a signal output line switching circuit for sequentially selecting from among the plurality of signal output lines according to a position of the selected image reading photoelectric conversion element (Tseng teaches that a EOS signal is transmitted to the next chip to enable the next chip for readout, col. 3, lines 60-67); a logic circuit for controlling the signal output line switching circuit (Tseng discloses master clock and control clock for controlling the timing of the imager); an output circuit for processing the photoelectric conversion signal that is transmitted through the selected signal output and then outputting a resulting signal, the output circuit being connected to the selected signal output line through the signal output line switching circuit (in Figure 10 Tseng discloses a differential amplifier for eliminating noise from the pixel signal using the dummy pixel signal, col. 4, lines 1-21); wherein the signal output line switching circuit switches to a signal output line corresponding to the next group from a signal output line currently selected after a last photoelectric conversion signal in a current group has been read and before a first photoelectric conversion signal in a next group is read (as previously mentioned Tseng discloses that once the last signal from a chip has been read, an EOS signal is sent to the next chip in sequence, col. 3, lines 60-67).

6. As for ***claim 11***, Tseng discloses a contact image sensor utilizing differential voltage pickoff. More specifically, Tseng discloses a plurality of image reading photoelectric conversion elements (pixels S_1-S_n) divided into a plurality of groups (grouping of the chips as shown in Figure 10); a first read selection circuit (shift register, col. 3, lines 54-57) for sequentially selecting the plurality of image reading photoelectric

conversion elements and reading a first photoelectric conversion signal from the selected image reading photoelectric conversion element; an first initialization selection circuit for sequentially selecting the plurality of image reading photoelectric conversion elements and initializing the selected image reading photoelectric conversion element (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel in sequence, col. 3, lines 59-60); a plurality of first signal output lines by way of which the first photoelectric conversion element signal is transmitted from the image reading photoelectric conversion elements, each of the plurality of signal output lines corresponding to and independently provided for each of the plurality of groups (as shown in Figure 10 each of the chips has an output line through which the photoelectric signal is transmitted); a plurality of dummy photoelectric conversion elements (d_1-d_n) divided into a plurality of second groups, each of the plurality of dummy photoelectric conversion elements shielded from light and forming an exclusive pair with one of the plurality of image reading photoelectric conversion elements by being arranged in close proximity thereto (col. 4, lines 1-21); a second read selection circuit (shift register also serves as the second read selection circuit since it operates to select and move charge out of the dummy pixels, col. 3, lines 54-57 and col. 4, lines 1-2) for sequentially selecting the plurality of dummy photoelectric conversion elements and reading a second photoelectric conversion signal from the selected dummy photoelectric conversion element; a second initialization circuit (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel in sequence, col. 3, lines 59-60) for sequentially selecting the plurality of dummy

photoelectric conversion elements and initializing the selected dummy photoelectric conversion element; a plurality of second signal output lines by way of which the second photoelectric conversion signal is transmitted from the plurality of dummy photoelectric conversion elements, each of the plurality of second signal output lines corresponding to and independently provided for each of the plurality of second groups (as shown in Figure 10 each of the chips has an output line through which the dummy signal is transmitted); a signal output line switching circuit for sequentially selecting from among the plurality of first signal output lines according to a position of the selected image reading photoelectric conversion element and also sequentially selecting from among the plurality of second signal output lines according to a position of the selected dummy photoelectric conversion element (Tseng teaches that a EOS signal is transmitted to the next chip to enable the next chip for readout, col. 3, lines 60-67); a logic circuit for controlling the signal output line switching circuit (Tseng discloses master clock and control clock for controlling the timing of the imager); an output circuit for processing the first and second photoelectric conversion signals transmitted through the selected first and second signal output lines respectively and then outputting a difference therebetween as a resulting signal, the output circuit being connected to the selected first and second signal output lines through the signal output line switching circuit (in Figure 10 Tseng discloses a differential amplifier for eliminating noise from the pixel signal using the dummy pixel signal, col. 4, lines 1-21); wherein, after a last image reading photoelectric conversion element in a first group currently selected and a last dummy photoelectric conversion element in a second group currently selected have

been read, and before a first image reading photoelectric conversion element in a first group subsequently selected and a first dummy photoelectric conversion element in a second group subsequently selected are read, the signal output line switching circuit switches selects one of the plurality of first signal output lines corresponding to the first group subsequently selected and one of the plurality of second signal output lines corresponding to the second group subsequently selected (as previously mentioned Tseng discloses that once the last signal from a chip has been read, an EOS signal is sent to the next chip in sequence, col. 3, lines 60-67. This is done for each of the chips and each of the chips includes both image reading pixels and dummy pixels.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (U.S. Patent No. 5,724,094)**.

8. As for ***claim 13***, Tseng discloses a contact image sensor utilizing differential voltage pickoff. More specifically, Tseng discloses a multiple chip IC for reading an image (Figure 10); a plurality of image reading photoelectric conversion elements (pixels S_1-S_n and d_1-d_n) divided into a plurality of groups (grouping of the chips as shown in Figure 10); a read selection circuit (shift register, col. 3, lines 54-57) for

sequentially selecting the plurality of image reading photoelectric conversion elements and reading a photoelectric conversion signal from the selected image reading photoelectric conversion element; an initialization selection circuit for sequentially selecting the plurality of image reading photoelectric conversion elements and initializing the selected image reading photoelectric conversion element (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel, col. 3, lines 59-60) ; a plurality of signal output lines by way of which the photoelectric conversion element signal is transmitted, each of the plurality of signal output lines corresponding to and independently provided for each of the plurality of groups (as shown in Figure 10 each of the chips has an output line through which the photoelectric signal is transmitted); a signal output line switching circuit for sequentially selecting from among the plurality of signal output lines according to a position of the selected image reading photoelectric conversion element (Tseng teaches that a EOS signal is transmitted to the next chip to enable the next chip for readout, col. 3, lines 60-67); a logic circuit for controlling the signal output line switching circuit (Tseng discloses master clock and control clock for controlling the timing of the imager); an output circuit for processing the photoelectric conversion signal that is transmitted through the selected signal output and then outputting a resulting signal, the output circuit being connected to the selected signal output line through the signal output line switching circuit (in Figure 10 Tseng discloses a differential amplifier for eliminating noise from the pixel signal using the dummy pixel signal, col. 4, lines 1-21); wherein the signal output line switching circuit switches to a signal output line corresponding to the next group

from a signal output line currently selected after a last photoelectric conversion signal in a current group has been read and before a first photoelectric conversion signal in a next group is read (as previously mentioned Tseng discloses that once the last signal from a chip has been read, an EOS signal is sent to the next chip in sequence, col. 3, lines 60-67). Furthermore, Tseng discloses the use of a clock signal. See column 4, lines 22-34. Inherently, the system would include a clock input terminal for inputting the clock signal into the device. Furthermore, as previously discussed Tseng discloses the use of an end of scan (EOS) feature, which operates as a start trigger. As shown in Figure 8, the EOS signal is input and output from each of the plurality of chips. Therefore each chip would include an input and output terminal for receiving the EOS signal.

Tseng, however, fails to specifically disclose the use of an A/D converter for converting the signal from the output circuit into a digital signal. Official Notice is taken as to the fact that it is well known in the art to convert analog signals into digital signals after readout from an image sensor. It is well known in the art that digital signals have advantages over analog signals in that they are less susceptible to interference, signal loss, and noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to convert the analog output of the device in Tseng to a digital signal so that it is less susceptible to noise.

9. With regard to ***claim 14***, Tseng discloses a contact image sensor utilizing differential voltage pickoff. More specifically, Tseng discloses a multiple chip IC for reading an image (Figure 10); a plurality of image reading photoelectric conversion

elements (pixels S_1-S_n) divided into a plurality of groups (grouping of the chips as shown in Figure 10); a first read selection circuit (shift register, col. 3, lines 54-57) for sequentially selecting the plurality of image reading photoelectric conversion elements and reading a first photoelectric conversion signal from the selected image reading photoelectric conversion element; an first initialization selection circuit for sequentially selecting the plurality of image reading photoelectric conversion elements and initializing the selected image reading photoelectric conversion element (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel in sequence, col. 3, lines 59-60); a plurality of first signal output lines by way of which the first photoelectric conversion element signal is transmitted from the image reading photoelectric conversion elements, each of the plurality of signal output lines corresponding to and independently provided for each of the plurality of groups (as shown in Figure 10 each of the chips has an output line through which the photoelectric signal is transmitted); a plurality of dummy photoelectric conversion elements (d_1-d_n) divided into a plurality of second groups, each of the plurality of dummy photoelectric conversion elements shielded from light and forming an exclusive pair with one of the plurality of image reading photoelectric conversion elements by being arranged in close proximity thereto (col. 4, lines 1-21); a second read selection circuit (shift register also serves as the second read selection circuit since it operates to select and move charge out of the dummy pixels, col. 3, lines 54-57 and col. 4, lines 1-2) for sequentially selecting the plurality of dummy photoelectric conversion elements and reading a second photoelectric conversion signal from the selected dummy photoelectric

conversion element; a second initialization circuit (shift register also serves as the initialization selection circuit, since it serves to reset the dark level of each pixel in sequence, col. 3, lines 59-60) for sequentially selecting the plurality of dummy photoelectric conversion elements and initializing the selected dummy photoelectric conversion element; a plurality of second signal output lines by way of which the second photoelectric conversion signal is transmitted from the plurality of dummy photoelectric conversion elements, each of the plurality of second signal output lines corresponding to and independently provided for each of the plurality of second groups (as shown in Figure 10 each of the chips has an output line through which the dummy signal is transmitted); a signal output line switching circuit for sequentially selecting from among the plurality of first signal output lines according to a position of the selected image reading photoelectric conversion element and also sequentially selecting from among the plurality of second signal output lines according to a position of the selected dummy photoelectric conversion element (Tseng teaches that a EOS signal is transmitted to the next chip to enable the next chip for readout, col. 3, lines 60-67); a logic circuit for controlling the signal output line switching circuit (Tseng discloses master clock and control clock for controlling the timing of the imager); an output circuit for processing the first and second photoelectric conversion signals transmitted through the selected first and second signal output lines respectively and then outputting a difference therebetween as a resulting signal, the output circuit being connected to the selected first and second signal output lines through the signal output line switching circuit (in Figure 10 Tseng discloses a differential amplifier for eliminating noise from the pixel

signal using the dummy pixel signal, col. 4, lines 1-21); wherein, after a last image reading photoelectric conversion element in a first group currently selected and a last dummy photoelectric conversion element in a second group currently selected have been read, and before a first image reading photoelectric conversion element in a first group subsequently selected and a first dummy photoelectric conversion element in a second group subsequently selected are read, the signal output line switching circuit switches selects one of the plurality of first signal output lines corresponding to the first group subsequently selected and one of the plurality of second signal output lines corresponding to the second group subsequently selected (as previously mentioned Tseng discloses that once the last signal from a chip has been read, an EOS signal is sent to the next chip in sequence, col. 3, lines 60-67. This is done for each of the chips and each of the chips includes both image reading pixels and dummy pixels). Furthermore, Tseng discloses the use of a clock signal. See column 4, lines 22-34. Inherently, the system would include a clock input terminal for inputting the clock signal into the device. Furthermore, as previously discussed Tseng discloses the use of an end of scan (EOS) feature, which operates as a start trigger. As shown in Figure 8, the EOS signal is input and output from each of the plurality of chips. Therefore each chip would include an input and output terminal for receiving the EOS signal.

Tseng, however, fails to specifically disclose the use of an A/D converter for converting the signal from the output circuit into a digital signal. Official Notice is taken as to the fact that it is well known in the art to convert analog signals into digital signals after readout from an image sensor. It is well known in the art that digital signals have

advantages over analog signals in that they are less susceptible to interference, signal loss, and noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to convert the analog output of the device in Tseng to a digital signal so that it is less susceptible to noise.

Allowable Subject Matter

10. Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 10 the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the initialization selection circuit initializes the selected image reading photoelectric conversion element during a last half of a period of the clock period and during a first half of a next clock period.

As for claim 12, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the first initialization selection circuit initializes the selected image reading photoelectric conversion element during a last half of a period of the clock period and during a first half of a next clock period and the second initialization selection circuit initializes the dummy photoelectric conversion element during a full period prior to the one period of the clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Mon.-Thurs, 7:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John M. Villecco
July 18, 2006